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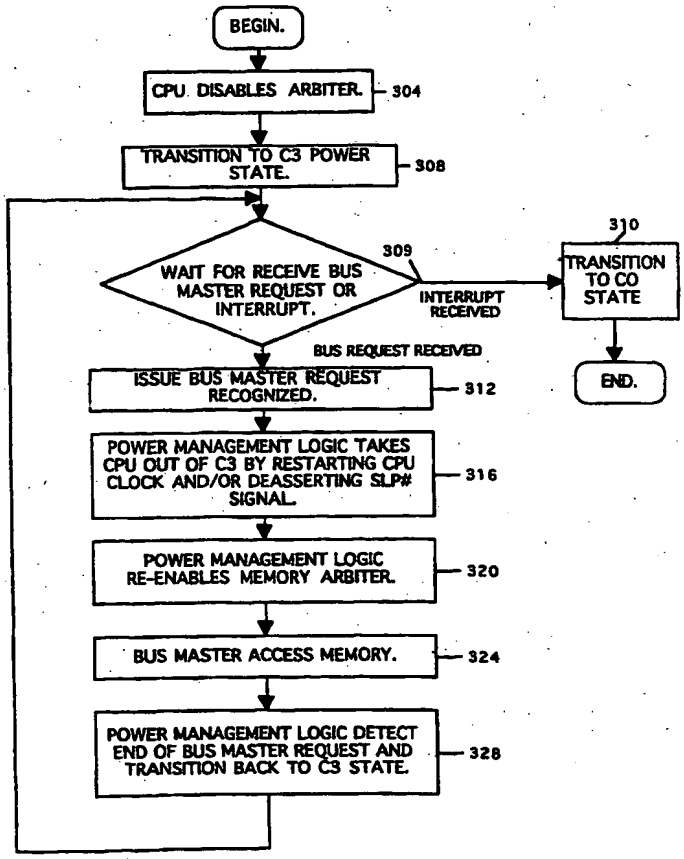
(54) Title: AUTOMATIC TRANSITIONING BETWEEN ACPI C3 AND C2 STATES

(57) Abstract

Minimizing power consumption of a processor and having at least three power states including a full power state, a first power conserving state, and a second power conserving state. The method involves placing the processor in a first conserving state (308), until a bus master requests snooping of a cache (309). Upon receipt of the request, the processor transitions directly into a second power conserving state (316), wherein the second power conserving state allows snooping of the cache. After snooping of the cache is completed, the processor returns directly to the first power conserving state from the second power conserving state (328).



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AUTOMATIC TRANSITIONING BETWEEN ACPI C3 AND C2 STATES

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates generally to reducing average power consumption by electronic devices. More particularly, the present invention relates to keeping the electronic devices in as low a power state as possible by turning off the electronic devices when various system caches do not need to be snooped.

2. DESCRIPTION OF RELATED ART

In recent years, portable battery operated computing devices have become increasingly popular. Portable computers enable workers and students to have computing power on demand at a variety of locations and not be limited by the power supply of a desktop machine. However, such portable computing devices are frequently limited by the amount of time that they can run on battery power without reconnection to an AC power supply. Thus, engineers are continuously trying to find ways of reducing the power consumption of various components of portable computers, including the central processing unit.

Keeping electronic devices such as a central processing unit, a memory controller or a memory in their lowest possible power state provides a number of benefits. For example, it allows battery operated machines to operate for longer periods of time between recharging. A reduction in power consumption also reduces thermal dissipation by the central processing unit. Reduced thermal dissipation allows the central processing unit to run at full speed for longer periods of time, while remaining within its thermal dissipation specifications. Reduced thermal dissipation also reduces the need for fans and other components used to prevent heat build-up in a computer. Finally, keeping the electronic device in a lower power state than could otherwise be achieved and reducing the number of transitions between power states improves system performance by reducing latencies caused by switching between designated power states.

A standard specification used in developing power management systems is the advanced configuration and power interface (ACPI) specification developed jointly by Intel Corporation of Santa Clara, California, Microsoft Corporation of Redmond, Washington and Toshiba Corporation of Tokyo, Japan. The ACPI specification is a key element in an operating system directed power management (OSPM). The goal of ACPI is to enhance power management functionality and robustness, as well as facilitating industry wide implementation of common power management features. The ACPI specification is a publicly available document and can be obtained from the Internet at www//http.teleport.com/~ACPI.

The ACPI defines a number of processor power states which are processor power consumption and thermal management states within a global working state. These processor states include a (i) CØ power state, (ii) C1 power state, (iii) C2 power state, and (iv) C3 power state. In the CØ power state, the processor executes instructions and is at full power. In the C1 and C2 power states, the processor is in a non-executing power state. However, the C2 power state uses less power than the C1 state. In the C1 and C2 power state, the processor still allows the bus to snoop the processor cache memory and thereby maintain cache coherency. The C3 power state offers improved power savings over the C1 and C2 power states. However, while in the C3 power state, the processor cache ignores any snoops. Thus, in the C3 state, the operating software is responsible for ensuring that the processor caches maintain coherency.

The CØ, C1, C2 and C3 power states of the ACPI map into various power states of commercial microprocessors. For example, with an INTEL® PENTIUM® processor, the CØ power state maps into a normal state in which all clocks are running, the C2 power state maps into a STOP GRANT state, and the C3 power state maps into a STOP CLOCK state.

In a traditional system, when a Peripheral Component Interconnect (PCI) peripheral signals that it needs to use the bus, the processor transitions from a C3 power state back to a CØ power state. As the system transitions back to the CØ power state, the central processing unit re-enables a bus arbiter.

A flow chart of a conventional implementation of a bus access is given in Figure 1. Before going to the C3 power state, the central processing unit (CPU)

disables an arbiter in step 104. In step 106, the CPU transitions to a C3 power state. When power management logic recognizes a bus master request, the power management logic causes the CPU to transition from a C3 power state back to a high powered CØ power state and generates an interrupt in step 108. Examples of conventional interrupts used in an INTEL® PENTIUM® processor include an Interrupt request ("INTR") or an active-low system management interrupt (SMI#). In the INTR or SMI# handler, the CPU which is now in a full power state re-enables the arbiter allowing the bus master to access the CPU's cache memory in step 112. The CPU also determines whether it can wait for the bus master to complete its transfers in step 116. If the CPU can wait for the bus master to complete its transfers, the CPU waits for completion of the transfers in step 120 and returns to step 104 to disable the arbiter. Disabling the arbiter returns the CPU to the C3 power state in step 106. Otherwise, if the CPU cannot wait for the bus master to complete its transfers, the CPU can be placed in a C2 power state in step 124.

The problem with the current method for handling bus arbiter requests is the unnecessary transition to the high-powered CØ power state. Transition to this power state is necessary in conventional systems to enable the CPU to disable and enable the arbiter in steps 112 and 124. Transitioning to the CØ power state consumes significantly more power than either the C3 or C2 power states. Thus, an improved method for handling bus master requests is needed.

SUMMARY OF THE INVENTION

The invention relates to a method and apparatus of minimizing power consumption in an electronic system which has a processor with at least three power states including a full power state, a first power conserving state, and a second power conserving state. The method comprises the steps of 1) placing the processor in a first conserving state, wherein the first power conserving state does not allow snooping of a cache memory; 2) detecting a bus master request to use a bus; 3) transitioning the processor directly into a second power conserving state, wherein the second power conserving state allows snooping of the cache; and 4) detecting when snooping of the cache is completed and returning the processor

directly to the first power conserving state from the second power conserving state.

BRIEF DESCRIPTION OF THE DRAWINGS

The advantages of the present invention will become more readily apparent to those ordinarily skilled in the art after reviewing the following detailed description and accompanying drawings, wherein:

Figure 1 is a flow diagram of the prior art method of handling CPU cache requests;

Figure 2 illustrates the transitions between processor power states in the ACPI specification as modified by the current invention;

Figure 3 is a flow diagram of one method of handling CPU cache requests involving transitions from the C3 or deep sleep power state to the C2 power state without powering the CPU to the CØ power state;

Figure 4 is one embodiment of a chip implementation for performing the method shown in flow diagram 3;

Figure 5 is a second embodiment of a hardware system capable of performing the flow diagram shown in Figure 3.

DETAILED DESCRIPTION OF THE INVENTION

A method and apparatus for conserving power in an electronic device is described. Figure 2 illustrates a modified ACPI processor power state diagram. The diagram includes both traditional transitions between power states and new transitions added by the present invention. All states, the CØ state 204, the C1 state 208, the C2 state 212 and the C3 state 216 are encompassed within a GØ working state 220. A GØ working state is defined by the ACPI specification as a computer state where the system dispatches user mode (application) threads. In the GØ working state, these threads are executed. In this state, devices (peripherals) are dynamically having their power states changed. Within this GØ state, a processor transitions between various processor power states including the CØ state 204, the C1 state 208, the C2 state 212, and the C3 state 216. In the CØ state, the processor is at full power.

The C1 state 208 defines a state in which the processor power state has the lowest latency. Aside from putting the processor in a non-executing power state, the C1 state 208 has no other software visible effects. The C2 state is a second non-executing power state which offers improved power savings over the C1 state 208.

The C3 power state 216 offers improved savings over both the C1 state 208, and the C2 state 212. While in the C3 state 216, the processor's caches maintain the respective cache states but ignore any snoops. Thus the operating system is responsible for ensuring that the caches maintain coherency.

In the standard ACPI specification, the transitions between states occur from the CØ state 204 along path 222 to the C1 state 208 and back to the CØ state along return path 224. Transitions also occur from the CØ state 204 to the C2 state 212 along path 226 and return to the CØ state 204 along path 228. Finally, transitions occur from the CØ state 204 along path 230 to the C3 state 216 and return to the CØ state along path 232. Stopping a clock is one method of generating a transition from the CØ state to the C2 state along path 226. An interrupt will result in a transition of the system from the C2 state 212 along a path 228 to the CØ state 204. In some processors, a transition from the CØ state 204 along path 230 to the C3 state 216 may be achieved by: 1) asserting a stop clock signal, 2) asserting a sleep signal, and 3) stopping the clocks. An interrupt or request for access will cause the processor to transition from the C3 state 216 along path 232 to the CØ state 204.

Applicant's invention adds two more paths along which a processor can transition directly between a C3 state 216 and a C2 state 212. By way of example, with an Intel® PENTIUM® family of processors, a transition from the C3 state 216 to the C2 state 212 along path 234 can be accomplished by restarting a clock and/or deasserting an optional SLP# signal. It should be noted that it is unnecessary to deassert a stop clock signal (STPCLK#) for this transition. Stopping a clock transitions the processor from a C2 state 212 to a C3 state 216 along path 232. In some processors, an optional sleep signal may also be asserted. In the preferred embodiment of the invention, the STPCLK# on the

Intel® PENTIUM® processor does not change while the processor is transitioning directly between the C3 state and the C2 state 212.

It should be recognized that although the description of this system will be described according to the ACPI specifications power states of CØ, C1, C2 and C3 for convenience, the invention is not limited by the ACPI specification. In general, for embodiments not following the ACPI specification, the C3 power state described in the specification will be equivalent to the lowest power state of a processor and should be considered to be a power state in which a CPU cannot maintain cache coherency. In this lowest power state, bus masters are prevented from accessing memory (because the CPU cannot snoop the cycles). In a system with an INTEL® PENTIUM® processor, the ACPI C3 power state is equivalent to a stop clock state. In some CPUs, the C3 power state is called a sleep or a deep sleep state. For purposes of this invention, the C3 power state is simply defined as a low power state in which cache coherency cannot be maintained, and thus, snooping of the cache memory is not permitted.

For purposes of this invention, the ACPI C2 power state is defined generally to be an intermediate power state between full power and the C3 power state. With an INTEL® PENTIUM® processor, the C2 power state is equivalent to the STOP GRANT state. In general the C2 power state allows snooping memory accesses and maintaining cache coherency. The CØ power state is defined for purposes of this invention as a full power state in which the CPU carries on its normal functions.

Figure 3 illustrates a method by which the bus master and power logic can access the cache of the CPU without raising the CPU to a full power state. In the flow chart of Figure 3, the CPU disables the arbiter in step 304 before transitioning into a lowest power or deep sleep C3 power state in step 308. The CPU remains in the C3 power state until a bus master request or interrupt is received in step 309. If an interrupt is received, the processor transitions to a CØ power state in step 310. If instead, a valid bus master request is recognized in step 312, the power management logic (typically a chipset) causes the CPU to transition from the C3 power state to a C2 power state in step 316. This transition

is usually accomplished by either restarting the CPU clock and/or deasserting the optional SLP# signal to an INTEL® PENTIUM® processor. It should be noted that with an INTEL® PENTIUM® processor, no INTR or SMI# interrupts need to be generated and transmitted to the CPU. Unlike prior systems, the CPU transitions directly from the C3 power state to the C2 power state without first going to the CØ (full power) state.

In order to allow bus master accesses, the power management logic chipset enables the memory arbiter in step 320. The memory arbiter may be found in a variety of memory controllers, similar to the one found in the Intel 82430TX. It should be noted that the CPU is not enabling the arbiter because the CPU is in a C2 power state and not executing instructions.

While the CPU is in the C2 power state, the bus master is allowed to access memory. As earlier defined, while the CPU is in a C2 power state (a low power state), the CPU can properly snoop the cycles and maintain cache coherency as done in step 324. After the bus master has completed its access of memory, the power management logic (chipset) detects the end of the bus master request and automatically transitions the CPU back to the C3 or deep sleep state in step 328. Thus, the memory access request issued while the CPU was in its lowest power C3 state did not cause the CPU to transition to the CØ or full power state. By avoiding the transition to the full power CØ state, the CPU saves both power and latency time by avoiding multiple transitions between states.

The above described method of handling bus requests while the CPU is in a very low power or deep sleep state may be accomplished by a variety of different apparatus. Figure 4 illustrates one embodiment of the present invention. A CPU 404 including a memory cache 408 is coupled to a memory controller 412 which helps direct flow of information to memory 416. The memory controller 412 is coupled to an ACPI or other power management system 420 via a high speed link 422. The power management logic 420 may include a bus interface, such as a Peripheral Component Interconnect (PCI), which connects a peripheral device 424 via a PCI or other appropriate bus 428. The peripheral 424 may transfer PCI requests to the ACPI power management unit 420 along bus 428. The power management unit 420 respond by transferring grant signals to the peripheral 424

along bus 428. The power management unit 420 also controls a clock generator 432 which clocks other chips in the system, such as the CPU, memory controller and memory.

A typical "wake-up" from a C3 power to a CØ power state occurs when a request such as a PCI request is transmitted to the power management unit 420, which responds by switching on the clock generator 432 turning the clocks on. Once appropriate delay times have been met, typically phase lock loop ("PLL") spin-up times (locking times), the CPU transitions to a C2 state appropriate for snooping of the cache memory. With an INTEL® PENTIUM® processor, the transition to a full power state (CØ) is accomplished by deasserting the stop clock (STPCLK#) signal such that the CPU starts executing instructions. In some processors, an optional sleep signal may also be used.

In the proposed embodiment, the power management unit 420 enables the clock generator 432 upon receipt of the PCI requests from peripheral 424. The start of the clock generator 432 starts the clocks to the memory controller 412 and the CPU 404. However, the CPU's stop clock signal (STPCLK#) is not deasserted. After all of the PLL's have stabilized, a power management unit 420 asserts a grant along PCI bus 428 to the peripheral 424, resulting in a memory cycle which can be snooped by the CPU 404. When the PCI request along PCI bus 428 goes inactive, the power management unit 420 deasserts the PCI grant signal and turns off the clocks to the memory controller 412 and to the CPU 404 by appropriately signaling clock generator 432.

Figure 5 shows an alternate system capable of implementing transitions directly from a deep sleep or C3 power state to a C2 or low powered snoop state without taking the CPU to a full power state. In the implementation shown, the CPU 504 including a cache 508 is connected to a memory controller 512. The memory controller includes a memory arbiter (not shown). The arbiter is coupled to a memory 516. A peripheral 524, such as a PCI peripheral, transmits a request to the memory controller to access memory. The request is routed to the power management unit 528 which in one embodiment may be a variant of the Intel PIIX4 chip.

The memory access request indicates to the power management unit 528 that the CPU should exit the C3 or deep sleep state. In response, the power management unit 528 starts a clock generator 532 which starts the clock to the CPU 504. In some CPUs an optional sleep signal may also be triggered to "wake up" the CPU. If CPU 504 is an INTEL® PENTIUM® processor chip, the stop clock signal is not deasserted. Thus, the CPU does not transition to a full power state. Instead, the CPU transitions directly to a C2 power state. When the power management unit 528 determines that the PLL clock has stabilized, a PLL OK signal is transmitted to the memory controller 512 indicating a grant signal may be transmitted from the memory controller to the peripheral 524. The peripheral 524 performs a memory cycle which allows snooping of the cache 508 of CPU 504. When snooping is complete, the memory request from the peripheral 524 goes inactive, the grants are deasserted and the clock to the CPU is turned back off.

Both embodiments of the ACPI power management unit, the power management unit 420 of Figure 4 or 528 of Figure 5 allow the CPU to transition from a deep sleep or C3 to an intermediate low power C2 power state without powering all the way back up to the fully powered CØ power state by including logic to start a clock to the CPU when a PCI request is received.

The present invention described herein may be designed in many different methods and using many different configurations. While the present invention has been described in terms of various embodiments, other embodiments may come to mind to those skilled in the art with departing from the spirit and scope of the present invention. The invention should therefore be measured in terms of the claims which follow.

What is claimed is:

1. A method of reducing power consumption in an electronic device having a first power conserving state and a second power conserving state, the method comprising the steps of:

placing the electronic device in a first power conserving state, said first power conserving state precludes snooping of a memory cache;

detecting a request to use a bus;

transitioning the electronic device directly from said first power conserving state into said second power conserving state, said second power conserving state allowing snooping of said memory cache; and

detecting when snooping of said memory cache is completed and returning said electronic device to said first power conserving state.

2. The method of claim 1 wherein said first power conserving state is a C3 power state and said second power conserving state is a C2 state of an Advanced Configuration and Power Interface specification.

3. The method of claim 1 wherein the transitioning of the electronic device from said first power conserving state to said second power conserving state includes the step of starting a clock which provides a timing signal to the electronic device.

4. The method of claim 3 further comprising the step of:

waiting for a phase lock loop spin-up delay before transitioning the electronic device to said second power conserving state; and

enabling an arbiter with an enabling circuit wherein the enabling circuit is separate from said central processing unit.

5. The method of claim 1 further comprising the steps of:

disabling an arbiter when said snooping of said cache is completed.

6. The method of claim 5 wherein said electronic device is a processor and said disabling step is executed by a second circuit, said second circuit is different from said processor.

7. A power efficient method of determining cache contents of an electronic device having at least three power states including the steps of:

recognizing a bus master request and restarting an electronic device clock thereby increasing the electronic device power consumption from a third power state to a second power state;

snooping a cache in said electronic device while said electronic device is in said second power state; and

returning said electronic device to said third power state immediately upon completion of said snooping of said cache.

8. The method of claim 7 further comprising the step of transmitting a disable signal from a power management logic to a bus arbiter disabling the bus arbiter.

9. The method of claim 8 further comprising the step of:

transmitting an enable signal from a power management unit independent of said central processing unit, said enable signal enabling said bus arbiter.

10. A system for minimizing the power consumption of an electronic device, said system comprising:

a cache memory in said electronic device, said electronic device having a low power state, an intermediate power state and a high power state;

a bus master which transmits a bus access request; and

a power management logic independent of said electronic device, said power management logic receives the bus master request and raises said electronic device from the low power state directly to the intermediate power state, said power management logic enabling a bus arbiter until the transfer of information from said bus master request has been completed.

11. The system of claim 10 further comprising:

an external clock which is switched on by said power management logic, the switching of said external clock raises said electronic device from the low power state to the intermediate power state.

12. The system of claim 10 wherein said power management unit deasserts a SLP# signal to move said electronic device from said high power state to the intermediate power state.

13. The system of claim 10 wherein said electronic device is a memory controller.

14. The system of claim 10 wherein said electronic device is a central processing unit.

15. The system of claim 14 wherein said power management unit includes a second central processing unit coupled to said power management unit, said second central processing unit clocked by said external clock and transitioning between a plurality of power states based on signals from said power logic unit.

16. The system of claim 14 wherein said low power state is a stop clock state of said central processing unit and said intermediate power state is a stop grant state of said central processing unit.

17. The system of claim 11 wherein said low power state is a C3 state and said intermediate state is a C2 state in a electronic device following the advanced configuration power interface specification.

18. A system for reducing the power consumption of a processing unit said system comprising:

means for storing information in said processing unit, said processing unit capable of operating in a plurality of power states including a low power state, an intermediate power state, and a full power state;

means for controlling the power state of said processing unit;

means for generating a bus access request, said means for generating a bus access request coupled to said means for controlling the power state of said processing unit, said means for controlling the power state of said processing unit transitions said processing unit from said low power state directly to said intermediate power state upon receipt of said bus access request and transitions said processing unit directly to said low power state upon completion of a bus access corresponding to said bus access request.

19. The system of claim 18 wherein said transition from said low power state to said intermediate power state is executed by restarting a clock.

20. The system of claim 18 wherein said restarting of said clock involves coupling an external clock to said processing unit.

21. A computer system comprising:

a power supply which provides power;

a processor coupled to said power supply and powered by said power supply, said processor including at least three power states, a deep sleep state, an intermediate power state and a full power state, and

a power management logic coupled to said processor, said power management logic causing said processor to transition directly to an intermediate power state from the deep sleep state when a request to snoop the central processing unit is received.

22. The system of claim 21 wherein said power supply is a battery.

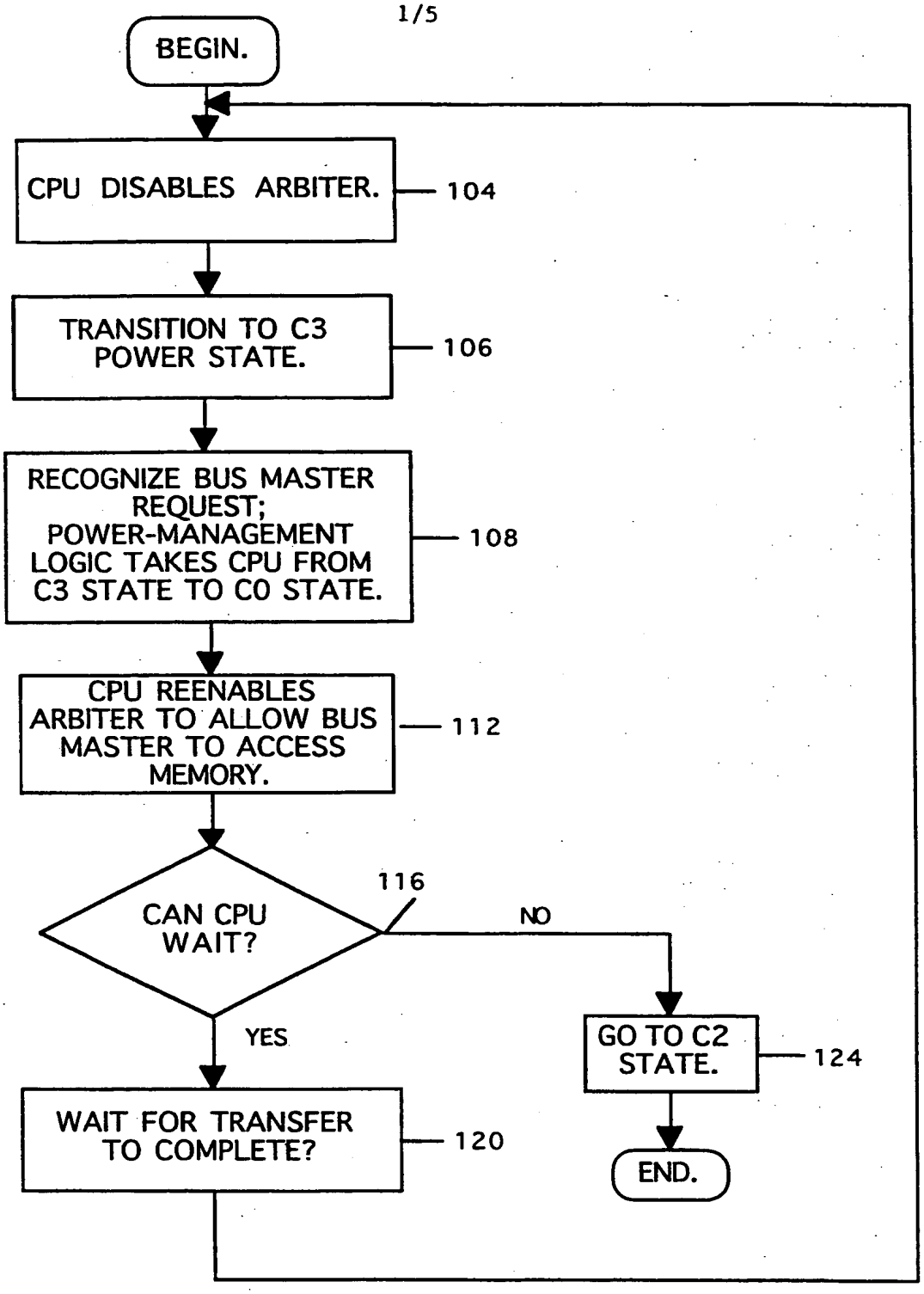
BEGIN.
CPU DISABLES ARBITER.
104
TRANSITION TO C3 POWER STATE.
106
RECOGNIZE BUS MASTER REQUEST; POWER-MANAGEMENT LOGIC TAKES CPU FROM C3 STATE TO C0 STATE.
108
CPU REENABLES ARBITER TO ALLOW BUS MASTER TO ACCESS MEMORY.
112
CAN CPU WAIT?
116
NO
YES
GO TO C2 STATE.
124
WAIT FOR TRANSFER TO COMPLETE?
120
END.

FIGURE 1.

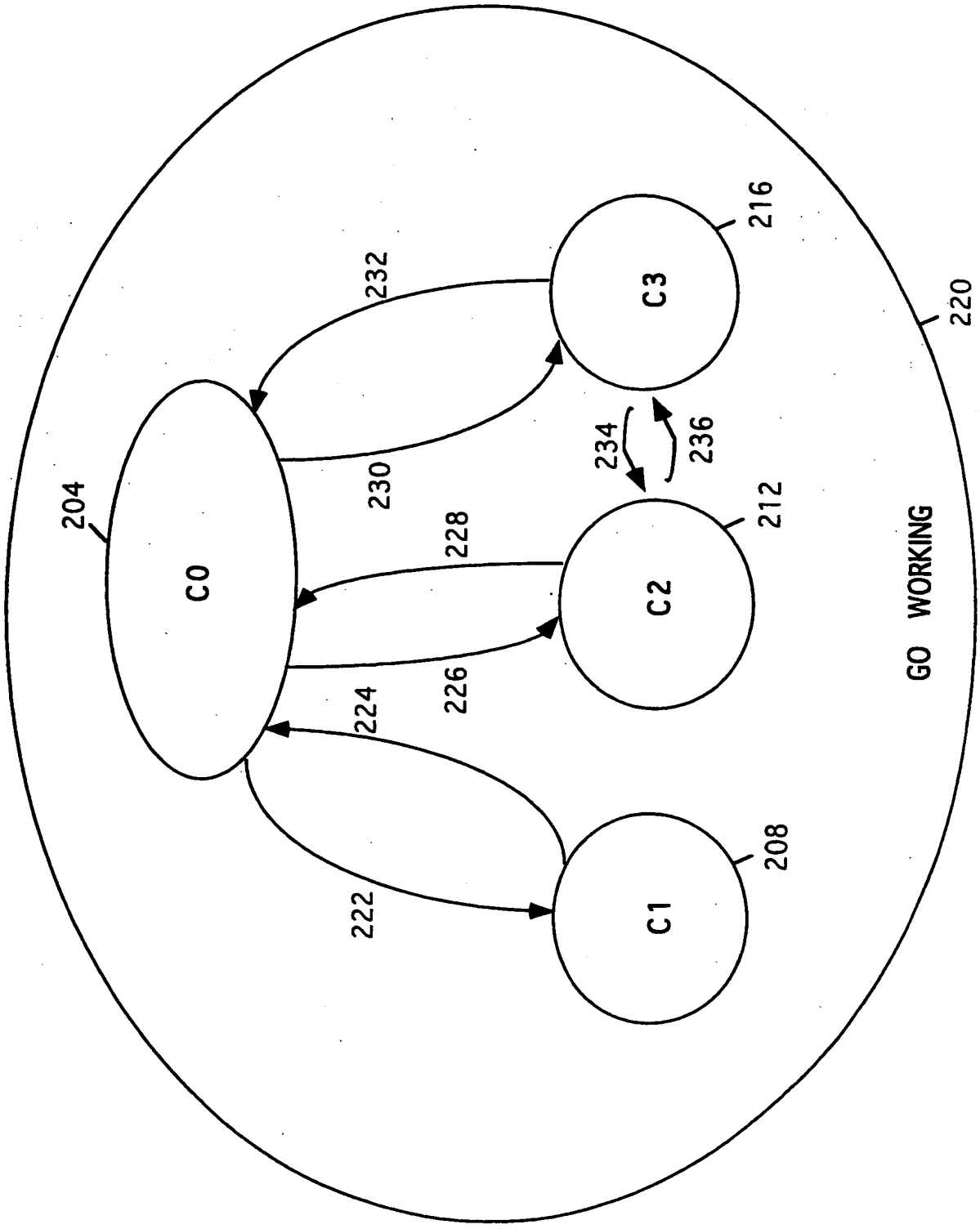
GO WORKING
220
C0
204
C1
208
C2
212
C3
216
222
224
226
228
230
232
234
236

FIGURE 2.

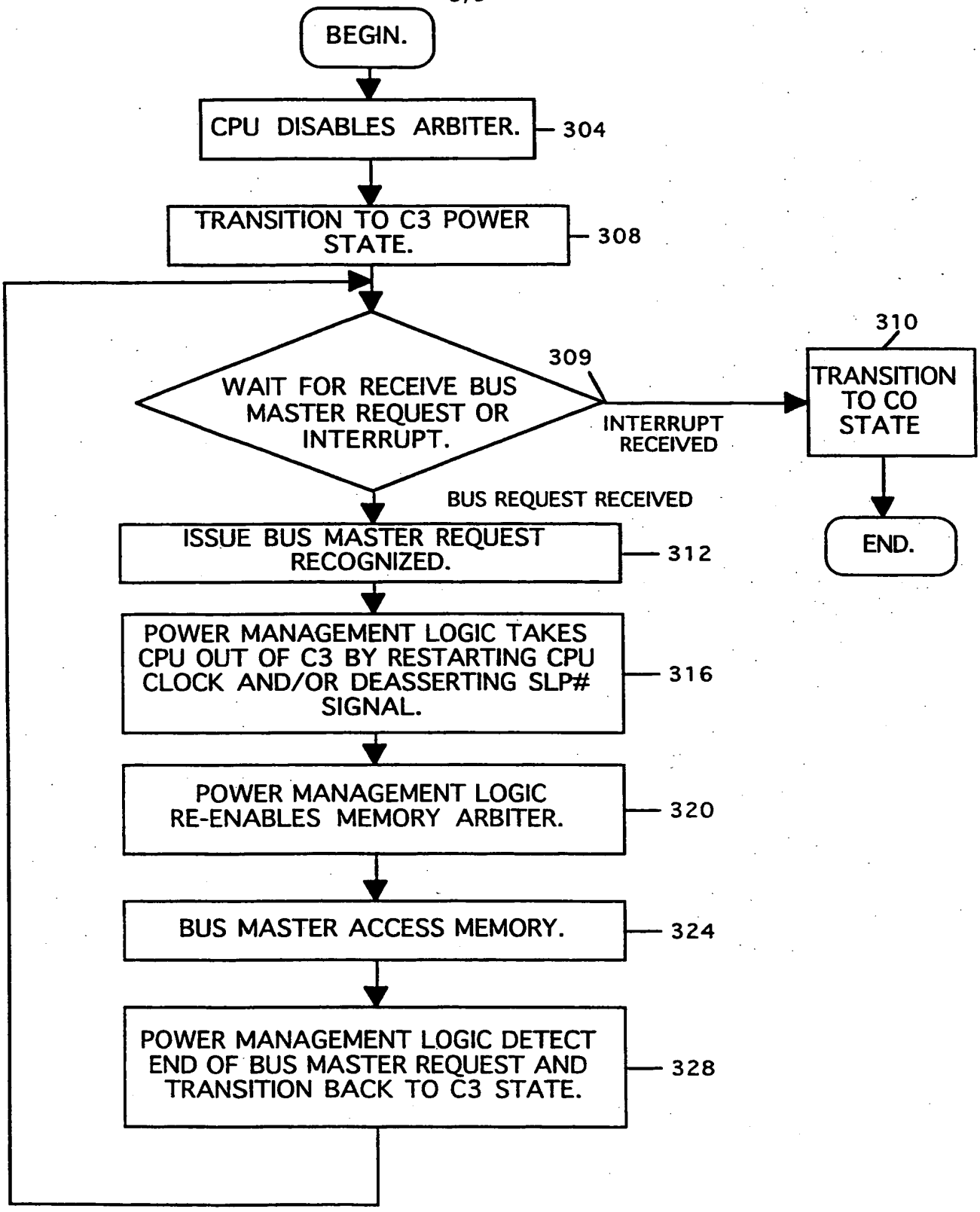
BEGIN.
CPU DISABLES ARBITER.
304
TRANSITION TO C3 POWER STATE.
308
WAIT FOR RECEIVE BUS MASTER REQUEST OR INTERRUPT.
309
INTERRUPT RECEIVED
310
TRANSITION TO CO STATE
END.
BUS REQUEST RECEIVED
ISSUE BUS MASTER REQUEST RECOGNIZED.
312
POWER MANAGEMENT LOGIC TAKES CPU OUT OF C3 BY RESTARTING CPU CLOCK AND/OR DEASSERTING SLP# SIGNAL.
316
POWER MANAGEMENT LOGIC RE-ENABLES MEMORY ARBITER.
320
BUS MASTER ACCESS MEMORY.
324
POWER MANAGEMENT LOGIC DETECT END OF BUS MASTER REQUEST AND TRANSITION BACK TO C3 STATE.
328

FIGURE 3.

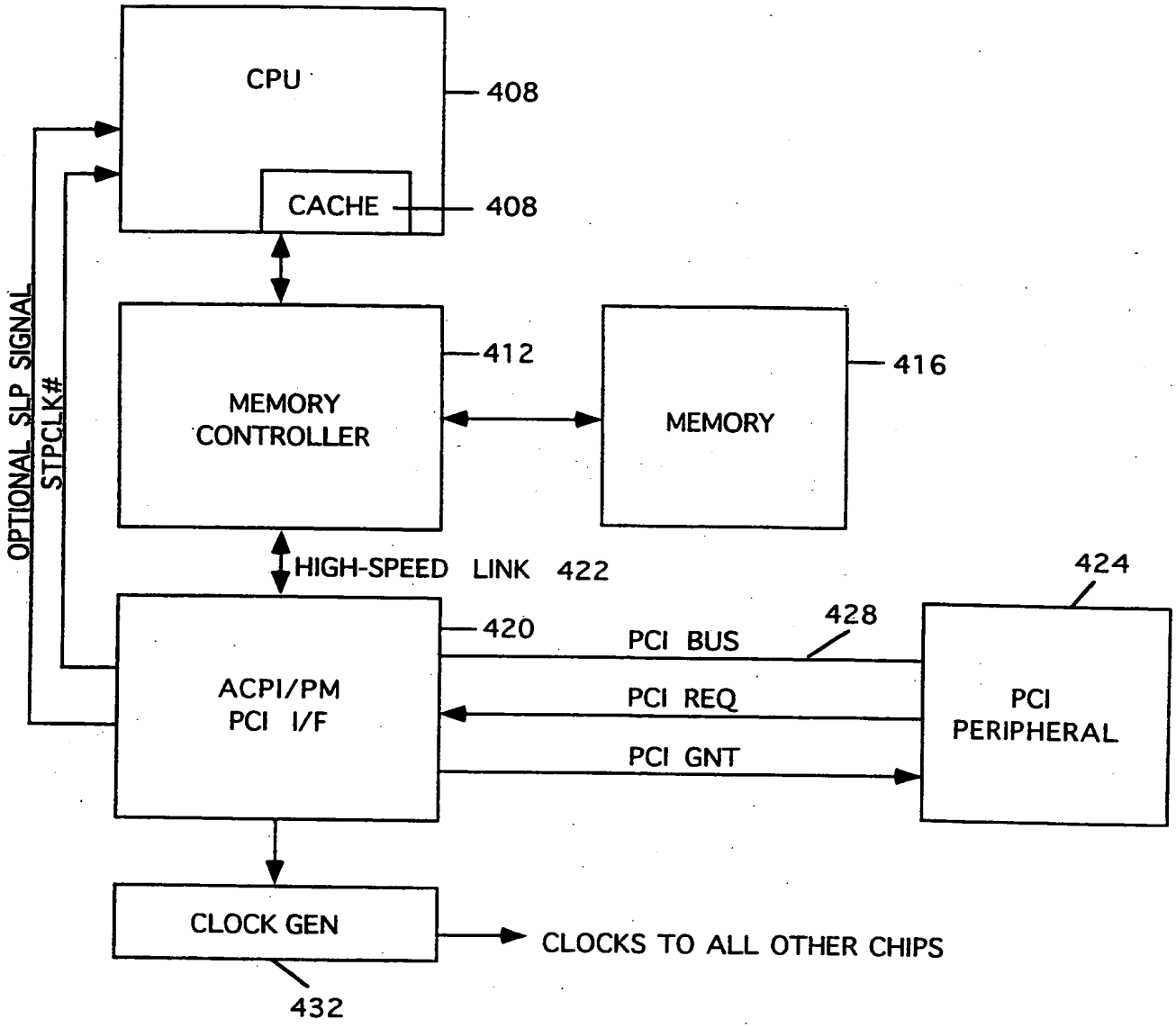

FIGURE 4.

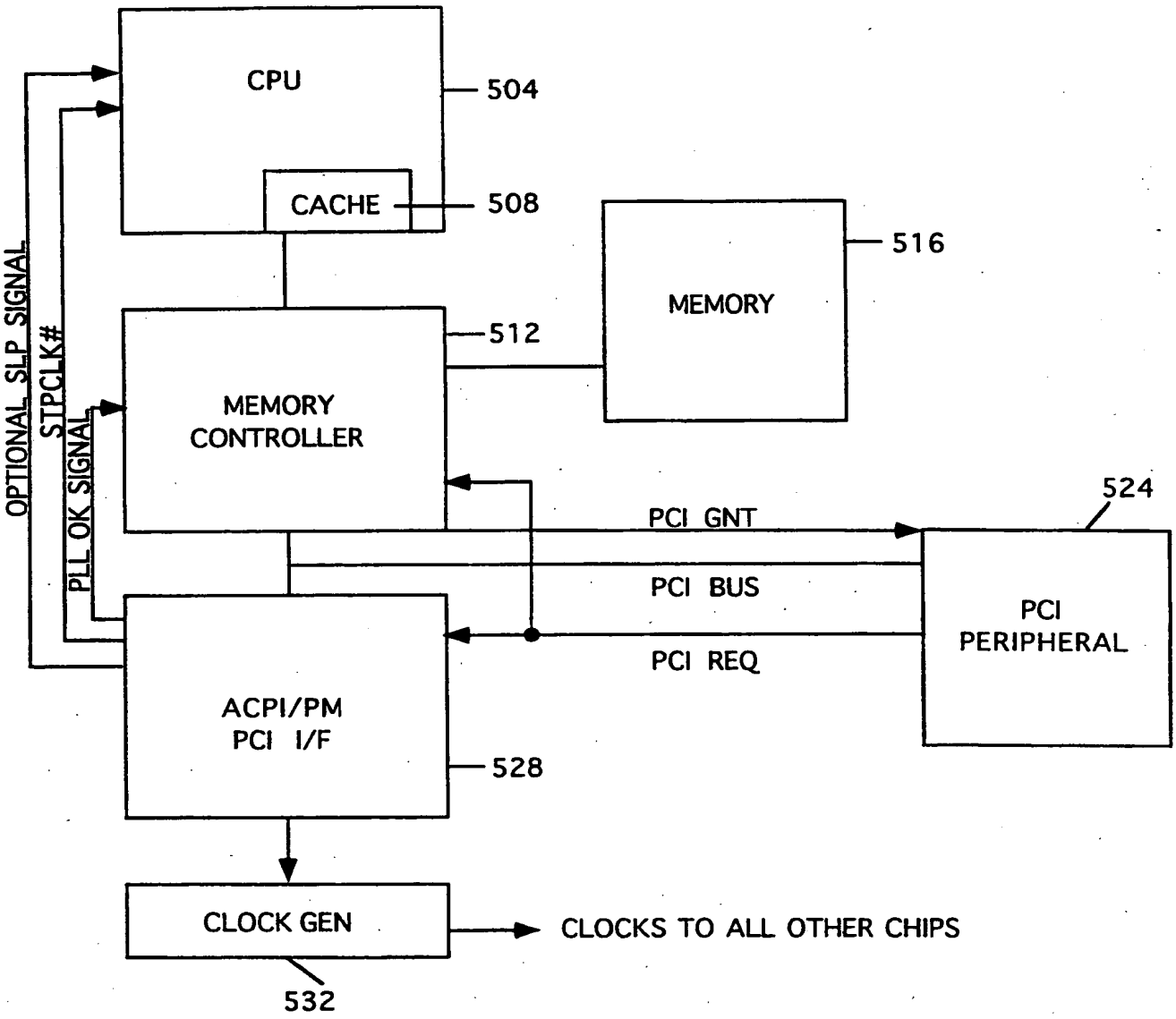
CPU
504
CACHE
508
516
MEMORY
512
MEMORY CONTROLLER
OPTIONAL SLP SIGNAL
STPCLK#
PLL OK SIGNAL
524
PCI GNT
PCI BUS
PCI REQ
PCI PERIPHERAL
ACPI/PM PCI I/F
528
CLOCK GEN
CLOCKS TO ALL OTHER CHIPS
532

FIGURE 5.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/01907

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G06F 1/32
US CL :395/750.04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/750.04, 750.01, 750.02, 750.03, 750.05, 750.06, 559, 560; 364/707

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,E --- Y,E	US 5,740,454 A (KELLY et al) 14 April 1998, col. 7, line 34 - col. 8, line 46.	1, 5, 6, 10, 12 - 14, 16, 18, 21-22 --- 2-4, 7-9, 11, 15, 17, 19, 20
A,P	US 5,713,029 A (KAISER et al) 27 January 1998, abstract.	1-22
Y	US 5,560,024 A (HARPER et al) 24 September 1996, col. 4, line 63 - col. 5, line 9.	3, 4, 7-9, 11, 17, 19, 20
Y	US 5,615,376 A (RANGANATHAN) 25 March 1997, abstract and col. 3, lines 31-38.	7-9

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
28 APRIL 1998	20 AUG 1998
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer SUMATI LEFKOWITZ Telephone No. (703) 308-7790

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/01907

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,E --- Y,C	US 5,721,935 A (DESCHEPPER et al) 24 February 1998, col. 7, line 34 - col. 8, line 46.	1, 5, 6, 10, 12-14, 16, 18, 21-22 --- 2-4, 7-9, 11, 15, 17, 19, 20
A,P	US 5,630,146 A (CONARY et al.) 13 May 1997, col. 19, line 64 - col. 20, line 67.	1-22
A,P	US 5,669,003 A (CARMEAN et al) 16 September 1997, abstract and col. 3, line 42 - col. 4, line 54.	1-22

Form PCT/ISA/210 (continuation of second sheet)(July 1992)*